BYPASS CIRCUITS FOR REDUCING PLASMA DAMAGE

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to a bypass circuit on a metal-oxide semiconductor (MOS) transistor, more specifically, to a bypass circuit for reducing plasma damage to a gate oxide of the MOS transistor.

2. Description of the Prior Art

A metal-oxide semiconductor (MOS) is a common electrical device used in integrated circuits. The MOS transistor is a unit, having four nodes, formed by a gate, a source and a drain. By utilizing channel effects generated by the gate of the MOS under different gate voltages, the MOS is often made to function as a digitalized solid switch applied on various integrated circuits of memory or logic devices.

Please refer to Fig.1 to Fig.4 of the cross-sectional views of manufacturing a MOS transistor according to the prior art. As shown in Fig.1, a silicon substrate 12, a gate oxide layer 14 and a gate 16 are formed, respectively, on a semiconductor wafer 10.

As shown in Fig.2, a first ion implantation process 18 is performed to form two doped areas, used as a lightly doped drain (LDD) 22 of the MOS transistor, located on either side of the gate 16 on the surface of the silicon substrate 12. The LDD 22 is also called

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a source-drain extension (SDE).

As shown in Fig.3, a spacer 24, composed of an insulating material, is then formed on either vertical wall of the gate 16. As shown in Fig.4, a second ion implantation process 26 is used to form two doped areas, used as a source 27 and a drain 28 of the MOS transistor, positioned on portions of the silicon substrate 12 adjacent to the spacer 24 to complete the manufacturing of the MOS transistor.

Please refer to Fig.5 of the cross-sectional view of performing a self-alignment silicide process on a MOS transistor.

The self-alignment silicide (salicide) process is often performed after the formation of the MOS transistor to reduce the contact resistance of each silicon surface on the MOS transistor. Therefore, a silicide layer 32 is formed on the surface of the gate 16, the source 27 and the drain 28 of the MOS transistor after the self-alignment silicide process.

However, a huge amount of ions accumulate in the gate 16 as a result of ultraviolet (UV) radiation during a plasma etching, ion bombardment and photo process. The accumulated ions may penetrate from the gate 16 into the gate oxide layer 14 and the silicon substrate 12 so as to cause the antenna effect and leading to the degradation of the gate oxide layer 14, or the so-called plasma process induced damage (PPID), to produce defective functioning of the MOS

transistor.

SUMMARY OF THE INVENTION

It is therefore a primary object of the present invention to provide a method for reducing plasma damage to a gate oxide of a metal-oxide semiconductor (MOS) transistor, in order to prevent the gate oxide layer of the MOS transistor from the plasma process induced damage (PPID).

In the preferred embodiment of the present invention, the MOS transistor is positioned on a substrate of a MOS semiconductor wafer. A dielectric layer is firstly formed to cover the MOS transistor on the substrate. An etching process is then performed to form a first contact hole through the dielectric layer to a gate on the surface of the MOS transistor, as well as to form a second contact hole through the dielectric layer to an n-well in the substrate. A bypass circuit and a fusion area are formed to electrically connect the MOS transistor and the n-well thereafter. The bypass circuit is composed of a metal layer and is positioned on the dielectric layer and on both the first and second contact holes, and the fusion area is composed of polysilicon or a narrow line. The fusion area is electrically cut off by performing a thermal process or by using a laser beam after the formation of the MOS transistor.

In the present invention, a bypass circuit is formed to electrically connect the MOS transistor and the

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n-well. It is therefore an advantage of the present invention over the prior art that accumulated ions in the gate oxide, as a result of ultraviolet (UV) radiation during the plasma etching, ion bombardment and photo process, is transferred to the n-well via the bypass circuit so as to neutralize the ions in the n-well. Thus, the antenna effect is prevented and the plasma process induced damage to the gate oxide is also reduced.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

BRIEF DESCRIPTION OF THE DRAWING

Fig.1 to Fig.4 are the cross-sectional views of manufacturing a MOS transistor according to the prior art.

Fig.5 is the cross-sectional view of performing a self-alignment silicide process on a MOS transistor according to the prior art.

Fig.6 to Fig.11 are the sectional views of a method for reducing plasma damage to a gate oxide of a MOS transistor according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Fig.6 to Fig.11 of the sectional views of a method for reducing plasma process induced

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damage (PPID) to a gate oxide of a MOS transistor according to the present invention. As shown in Fig.6, a silicon substrate 42, a gate oxide layer 44 and a gate 46 are formed, respectively, on a semiconductor wafer 40. An n-well 50, isolated from the MOS transistor by a shallow trench insulator (STI) 70, is set in a portion of the substrate 42 a distance away from the gate 46.

As shown in Fig.7, a first ion implantation process 48 is performed to form two doped areas, used as the lightly doped drain (LDD) 52 of the MOS transistor, on either side of the gate 46 on the surface of the silicon substrate 42. The LDD 52 is also called a source-drain extension (SDE).

As shown in Fig.8, a spacer 54, composed of an insulating material, is then formed on either vertical wall of the gate 46. As shown in Fig.9, a second ion implantation process 56 is performed to form two doped areas, used as a source 57 and a drain 58 of the MOS transistor, in a portion of the silicon substrate 42 adjacent to the spacer 54 to complete the manufacturing of the MOS transistor.

As shown in Fig.10, a dielectric layer 60 is formed to cover the MOS transistor. An etching process is then performed to form a first contact hole 62 through the dielectric layer 60 to the surface of the MOS transistor, as well as to form a second contact hole 64 through the dielectric layer 60 to the n-well 50 in the silicon substrate 42. As shown in Fig.11, a

bypass circuit 66, a portion of a metal interconnect layer, and a plug composed of tungsten (W) or other conductive materials, are positioned on the dielectric layer 60 and the first and second contact holes 62 and 64. A fusion area, electrically connecting with the bypass circuit 66, is formed to electrically connect the MOS transistor and the n-well thereafter. A deposition and a photo-etching-process (PEP) is then performed to form the metal interconnect layer and to define the patterns of the bypass circuit 66. A deposition and the photo-etching-process is again performed to form a fusion area 68 of the bypass circuit 66 on the dielectric layer 60 to electrically connect the MOS transistor and the n-well 50. Ions accumulated in the gate oxide as a result of ultraviolet (UV) radiation during the subsequent plasma etching, ion bombardment and photo process is thus transferred to the n-well 50 via the bypass circuit 66 to neutralize the ions in the n-well 50 and reduce plasma damage to the gate oxide layer 44.

The fusion area 68 of the bypass circuit 66 on the dielectric layer 60 can also be formed before the formation of the metal interconnect layer which electrically connects with the MOS transistor, fusion area 68 and the n-well 50. Also, the fusion area 68 can also be formed during the formation of the gate 46 by performing the photo-etching-process used to define patterns of the gate 46 and to form both the gate 46 and the bypass circuit 66. The fusion area 68 is electrically cut off by performing a thermal process or by using a laser beam after the formation of the

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MOS transistor.

In comparison with the prior art, the present invention electrically connects the MOS transistor and the n-well via a bypass circuit. Consequently, ions accumulated in the gate oxide layer as a result of ultraviolet (UV) radiation during the plasma etching, ion bombardment and photo process can be transmitted to the n-well via the bypass circuit so as to neutralize the ions in the n-well. Thus, the antenna effect caused by the penetration of ions from the gate into the silicon substrate to lead to the degradation of the gate oxide layer, can be prevented and the plasma process induced damage (PPID) to the gate oxide can also be reduced to ensure the proper functioning of the MOS transistor.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.